048/2025

PART – II

Total Number of Questions : 40	Maximum Marks : 200	Time : 3 Hours

INSTRUCTIONS (നിർദ്ദേശങ്ങൾ)

1. Question cum Answer Booklets are processed by electronic means. The following instructions are to be strictly followed to avoid invalidation of answer scripts.
(ചോദ്യവും ഉത്തരവും അടങ്ങുന്ന ഈ ബുക്ക് ലെറ്റുകൾ ഇലക്ട്രോണിക് സാങ്കേതിക വിദ്യയുടെ സഹായത്തോടുകൂടെ മൂല്യനിർണ്ണയം നടത്തുന്നതിനാൽ ഇവ അസാധുവാകാതിരിക്കുവാൻ താഴെപ്പറയുന്ന നിർദ്ദേശങ്ങൾ പൂർണ്ണമായും പാലിക്കുക.)

2. The first page of this question cum Answer Booklet is an OMR data Sheet (Part I). All entries in the OMR sheet are to be made with blue or black ball point pen only.
(ഈ പുസ്തകത്തിന്റെ ഒന്നാമത്തെ പേജ് ഒരു ഒ.എം.ആർ. ഡാറ്റാ ഷീറ്റാണ് (പാർട്ട് I). ഇത് നീലയോ, കറുപ്പോ നിറത്തിലെ ബോൾ പോയിന്റ് പേന ഉപയോഗിച്ച് മാത്രമേ പൂരിപ്പിക്കാവൂ.)

3. Make sure that register number is bubbled correctly and completely; no correction is permitted.
(രജിസ്റ്റർ നമ്പർ രേഖപ്പെടുത്തുന്നതിനുള്ള കുമിളകൾ കൃത്യമായും പൂർണ്ണമായും കറുപ്പിച്ചിട്ടുണ്ടെന്ന് ഉറപ്പു വരുത്തുക. തിരുത്തലുകൾ അനുവദനീയമല്ല.)

4. Do not tamper the bar code printed on the OMR sheet and subsequent pages. Tampering of bar code will result in the invalidation of this booklet.
(ഈ പുസ്തകത്തിൽ എവിടെയും പ്രിന്റ് ചെയ്തിരിക്കുന്ന ബാർ കോഡിൽ ഒരു കാരണവശാലും തിരുത്തലുകളോ, മാർക്കുകളോ പാടില്ല. ഇതിനു വിരുദ്ധമായി ചെയ്യുന്ന പക്ഷം ഈ പുസ്തകം അസാധുവാകുന്നതാണ്.)

5. Answers should be written with blue or black ball point pen only.
(ഉത്തരങ്ങൾ നീലയോ, കറുപ്പോ നിറത്തിലെ ബോൾ പോയിന്റ് പേന ഉപയോഗിച്ച് മാത്രമേ എഴുതാവൂ.)

6. Do not write anything outside the margin of space provided for writing the answer and write only one line of answer between two lines.
(പുസ്തകത്തിൽ ഉത്തരം എഴുതുവാൻ നൽകിയിരിക്കുന്ന സ്ഥലത്തിനു വെളിയിൽ യാതൊന്നും തന്നെ എഴുതുവാൻ പാടില്ല. രണ്ടു വരകൾക്കിടയിൽ ഒരു വരി ഉത്തരം മാത്രമേ എഴുതുവാൻ പാടുള്ളൂ.)

7. Rough work should be done only in the specific page provided with.
(റഫ് വർക്കുകൾ ഇതിനായി നൽകിയിരിക്കുന്ന പേജിൽ മാത്രമേ ചെയ്യുവാൻ പാടുള്ളൂ.)

1. How must the two transistor junctions be biased for proper transistor amplifier operation? What is the source of leakage current in a transistor? For CB configuration, determine α_{dc} if $I_E = 2.7\,mA$ and $I_B = 19\mu A$. (5 Marks)

2. What is the significant difference in the construction of an enhancement type MOSFET and a depletion type MOSFET? Sketch the basic construction of an n-channel depletion type MOSFET, apply the proper drain-to-source voltage and sketch the flow of electrons for $V_{GS} = 0V$. (5 Marks)

3. Explain the principle of operation of thermistor. A thermistor has a resistance temperature coefficient of –5% over a temperature range of 35°C to 60°C. If the resistance of the thermistor is 90 Ω at 35°C, what is the resistance at 45°C. (5 Marks)

4. With a neat sketch, explain the working principle of Hall effect transducer. List any two applications of Hall effect transducer. A Hall effect transducer is used for the measurement of magnetic field of 0.7 Wb/m^2. The 2mm thick slab is made of Bismuth for which the Hall's coefficient is $-1\times10^{-6}\,\mathrm{Vm/(A-Wbm^{-2})}$ and the current is 4A. Determine the output voltage. (5 Marks)

5. A combinational logic circuit with three inputs (A, B, C) and one output (F) is defined by the Boolean function $F(A, B, C) = \sum(0,3,5,6)$. Examine the feasibility of implementing this Boolean function $F(A, B, C)$ using a 4:1 multiplexer. If it is possible, provide a detailed circuit diagram that illustrates how to connect the input variables (A,B,C) to the select and data lines of the 4:1 multiplexer using any necessary logic gates. If it is not possible, explain the reason why. (5 Marks)

6. A digital system utilizes a cascaded arrangement of single-digit BCD adders to perform additions on multi-digit BCD numbers.

   (a) Use your understanding of BCD addition and carry propagation to explain how the carry-out signal from one single-digit BCD adder stage is utilized as the carry-in signal for the next higher-order BCD adder stage when adding multi-digit BCD numbers.

   (b) Analyze a scenario where two 2-digit BCD numbers, 39 and 18, are added using two cascaded single-digit BCD adders. Trace the flow of data and carry signals through both adder stages, highlighting the intermediate binary sums and the application of the correction logic in each stage. (5 Marks)

7. A digital system requires a modulo-1024 counter (which can be implemented using a 10-bitcounter) to be clocked at a frequency of 10 MHz. The design team is considering using either an asynchronous (ripple) counter built with commercially available J-K flip-flops or a synchronous counter.

   (a) Analyze the potential limitations of using an asynchronous counter with J-K flip-flops that have a maximum propagation delay of 15 ns each for this application. Specifically, calculate the maximum operating frequency achievable with this asynchronous design and discuss whether it meets the system requirement of 10 MHz.

   (b) Why would a synchronous counter be preferred over an asynchronous counter for a 10 MHz application, considering that the flip-flops used in either design have a maximum propagation delay of 15 ns?

(5 Marks)

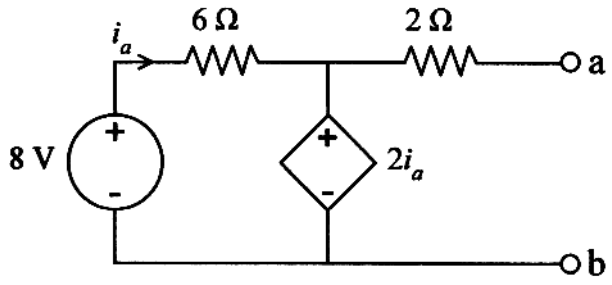
8. A student is using a two-input TTL NAND gate IC in a digital logic experiment. They connect both inputs of one of the NAND gates to a HIGH logic level (+5V).

   (a) Draw the internal circuitry of a standard TTL NAND gate to predict the state (HIGH or LOW) of the output of this NAND gate under these input conditions. Explain your answer by detailing the conduction (ON/OFF) stages of the relevant transistors within the NAND gate and how these states lead to the predicted output level.

   (b) Analyze the current flow within the TTL NAND gate when both inputs are held HIGH. Describe the states (ON or OFF) of the key transistors in the output stage (totem-pole configuration) and explain the path of current that determines the output voltage level. What is the expected approximate voltage level at the output in this state?

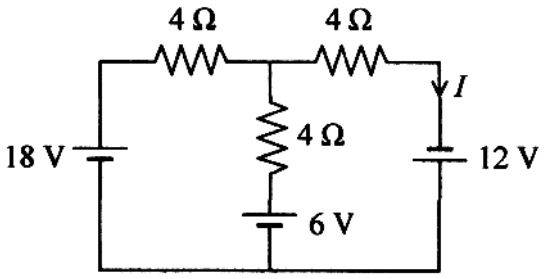
(5 Marks)

9. Find Norton's equivalent circuit parameters of the given circuit. (5 Marks)

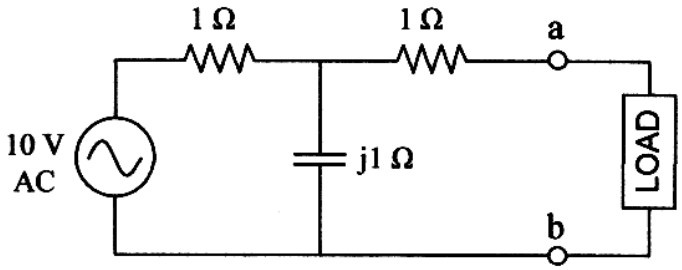


10. Using superposition method, find the current I in the circuit below.

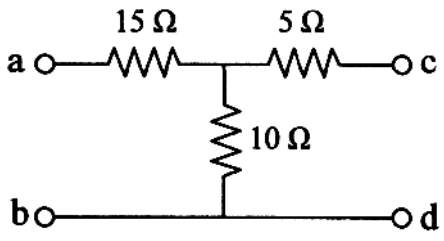
(5 Marks)



11. For the given circuit, determine the value of load impedance so that maximum power is transferred through the terminals *a* and *b*. (5 Marks)



12. Find the Z parameters of the given network. State whether reciprocity condition is satisfied in the network. (5 Marks)



13. Input to a linear delta modulator is a sinusoidal signal whose frequency can vary from 200 hz to 4000 hz. The input is sampled at 8 times the Nyquist rate. The peak amplitude of the sinusoidal signal is 1 volt.

(a) Determine the minimum value of the step size in order to avoid slope overload when the input signal frequency is 800 hz.

(b) What is the peak amplitude of the input signal, to just overload the modulator, when the input signal frequency is 200 hz?

(c) Is the modulator overloaded when the input signal frequency is 400 hz? (5 Marks)

14. For an amplitude modulation double side Band full carrier wave, with a peak unmodulated carrier voltage of 10V and load resistance of 10 ohm, the modulation index is 0.5. Assume that both the carrier and modulating signals are sinusoidal.

(a) Write the time equation for the modulated signal.

(b) Find the rms power of the carrier and total rms power of modulated wave. (5 Marks)

15. Explain the generation and detection of coherent binary PSK signals. (5 Marks)

16.

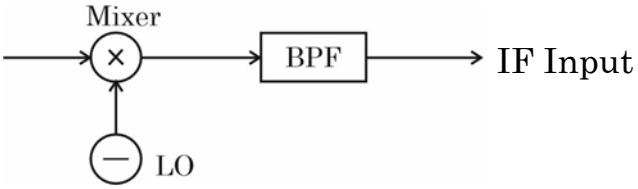


Figure shows the first stage of a super heterodyne receiver. The desired input signal is at a frequency of 700 Mhz. The LO freq is 1 Ghz. The mixer is an ideal multiplier with a gain independent of frequency. A BPF is used to select IF output at 300 Mhz.

(a) What is the image freq. of desired input?

(b) A LPF can be used before the mixer to reject the image frequency. If a perfect rejection of the image is desired, what type of LPF should be employed?

(c) The input in figure is corrupted by an undesired 750 Mhz signal, which has the same amplitude as those of desired signal at 700 Mhz. Let the BPF be of second order. At the BPF output, the undesired signal should be 20 dB below the desired signal. Calculate the Q required for the BPF. (5 Marks)

17. What is the fundamental period of the discrete time signal? (5 Marks)

$$x[n] = e^{j\left(\frac{2\pi}{3}\right)n} + e^{j\left(\frac{3\pi}{4}\right)n}$$

18. If $x_1(t) = 100\cos(2\pi\, 1000\, t)$ and $x_2(t) = 50\sin(2\pi\, 500\, t)$. What is the Nyquist sampling frequency of the signal $x_3(t) = x_1(t).x_2(t)$? (5 Marks)

19. Using the bilinear transformations, $s \approx \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$, where T is the sampling period, obtain the z-domain transfer function for a low pass filter with a cutoff frequency of 100 rad/s at a sampling frequency of 50 Hz. The transfer function of the low pass filter is $G(s) = \frac{100}{s+100}$. (5 Marks)

20. Consider a 16-bit binary number $b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5\, b_4b_3b_2b_1b_0$ whose Q1.15 representation is given by the following expression,

$$-2^0 \times b_{15} + 2^{-1} \times b_{14} + 2^{-2} \times b_{13} + \ldots + 2^{-15} \times b_0$$

What will be the Q1.15 representation of the hexadecimal number A000 be? (5 Marks)

21. Compare MOSFETs with BJTs. (5 Marks)

22. Substantiate the behavior of frequency response of an RC coupled amplifier considering. (5 Marks)
    (a) low frequency region
    (b) mid frequency range
    (c) high frequency range.

23. Compare series current feedback and series voltage feedback topologies. (5 Marks)

24. Differentiate between dc load line and ac load line in the analysis of a BJT with emitter resistor and emitter bypass capacitor. (5 Marks)

25. Explain internal program memory and data memory of 8051. (5 Marks)

26.

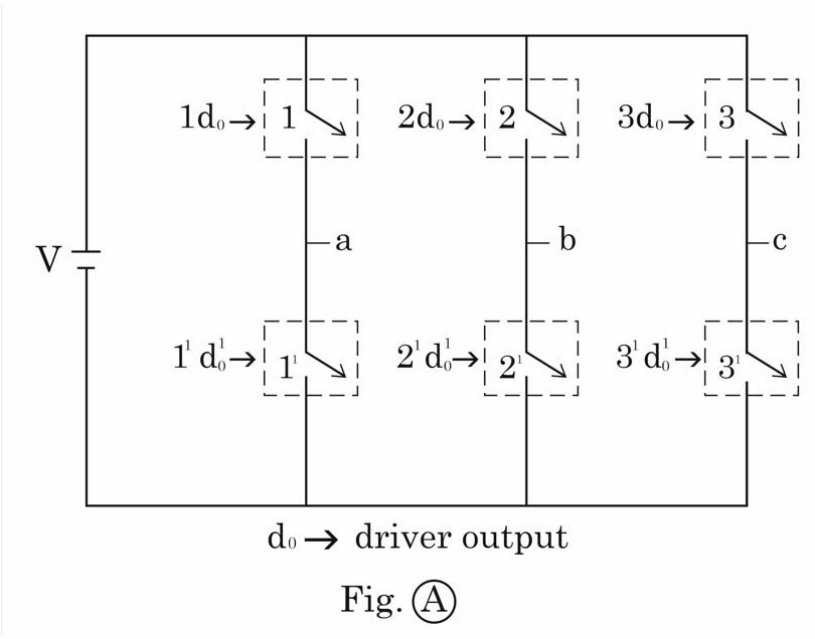


Fig. Ⓐ

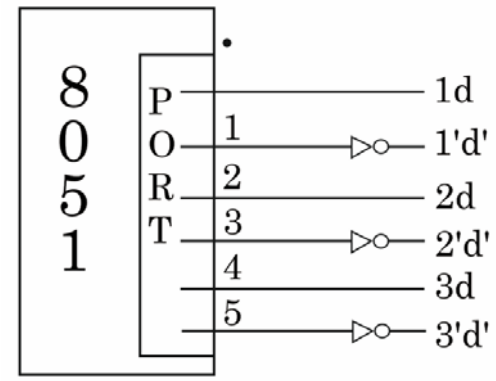
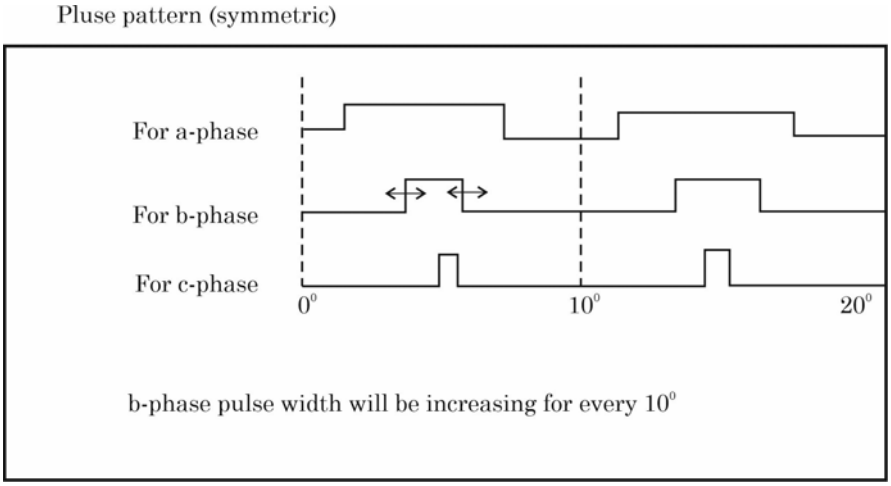


Fig. Ⓑ

1d, 2d, 3d → driver for 1, 2, 3
1'd', 2'd', 3'd' → driver for 1', 2', 3'

Fig A is a 3ϕ voltage source inverter (VSI) and it is controlled via 8051 processor. Write an algorithm to generate pulses for the inverter. Pulse pattern is explained below.

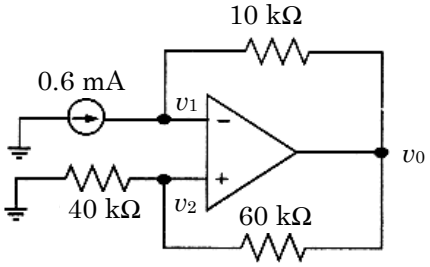


Generated pulses from the processor will be fed to the driver and the driver circuit amplify the pulse and used to turn the status of the power device in the inverter to "ON" or "OFF" state. (5 Marks)

27. Explain the addressing modes of 8051. (5 Marks)

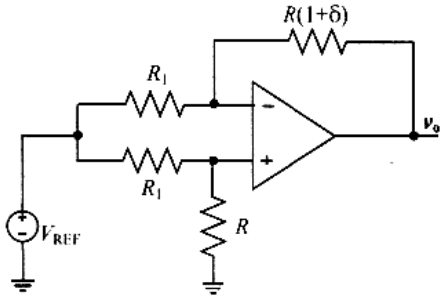
28. Explain the data processing instructions pertaining to 'ARM ' processor. (5 Marks)

29. Determine the voltage v_1, v_2 and v_0 for the circuit shown below. (5 Marks)



30. Design an op-amp based amplifier circuit with two inputs and two outputs that can provide the sum $(V_{sum} = v_1 + v_2)$ and the difference $(V_{dif} = v_1 - v_2)$. Where v_1 and v_2 are two inputs respectively. Use only two op-amps and minimum number of components. (5 Marks)

31. A typical strain gauge signal conditioning circuit is shown below. Prove that the output v_0 of the circuit is linear with respect to the δ, where δ is the ratio of change in resistance to the original resistance. (5 Marks)



32. Design a three-input instrumentation amplifier and derive its output in terms of the input voltages. (5 Marks)

33. Find the step response of a system with the transfer function, $G(s)=\dfrac{10}{s+20}$ if the magnitude of the step input is 0.1 unit. (5 Marks)

34. The transfer function $F(s)$ of a system is given by $F(s)=\dfrac{s+k_2}{s^4+2s^3+2s^2+2s-k_1}$ where k_1 and k_2 are real numbers. With suitable justifications find all possible values that k_1 and k_2 can take so that the system will always remain stable. (5 Marks)

35. For the state space representation of the system given by

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}-\delta & 0\\ 0 & \delta\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}1\\ 1\end{bmatrix}u \quad y=\begin{bmatrix}1 & 1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+u$$

obtain the transfer function in terms of δ , where δ is a constant real number. (5 Marks)

36. With suitable justifications obtain the condition to be satisfied by α and ϕ, for the given system described by

$$\ddot{x}_1 = 2x_1 + 5x_2$$
$$\ddot{x}_2 = 4x_1 + 7x_2 + \alpha u$$
$$y = \phi x_1$$

to be both controllable and observable, use Kalman's test. Here, x_1 and x_2 are state variables, u is the control input, y is the output, α and ϕ are real numbers. (5 Marks)

37. How are reflex Klystron oscillators are different from other cavity resonators? (5 Marks)

38. Explain the structure and working principle of an Inverted-F Antenna (IFA) used in mobile phones. (5 Marks)

39. The TCP/IP protocol suite is the foundation of modern internet communication. Discuss its layered architecture, explaining the functionalities of each layer. How does the suite ensure reliable data transmission across networks and what mechanisms are employed to handle errors, congestion and security threats? (5 Marks)

40. What are the key factors contributing to signal attenuation in optical fibers, and what advanced strategies and technologies can be employed to mitigate these losses effectively? (5 Marks)
